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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/525,921
Filing Date: February 25, 2005
Appellant(s): ROSKER ET AL.

Robert B. Levy (28,234)
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 12/04/2007 appealing from the Office action mailed 07/18/2007.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

US Pat 6,792,507	Chiou et al	9-2004
US Pub 2002/0184460	Tremblay et al	12-2002

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims **1-2, 4-12, 15-16** are rejected under 35 U.S.C. 102(e) as being anticipated by Chiou et al. (United States Patent 6,792,507).

As per Claim 1, Chiou et al. discloses, "a storage mechanism for storing content" as **["storing data on computers" (Col 1, Line 7)]** "at least one local cache

storage unit for mirroring at least a portion of the content stored on the storage mechanism" **[Chiou et al. discloses this limitation as "Caching is a technique of mapping frequently used data from a slow storage device, in which it is typically stored, to a higher speed storage device to achieve data access performance gains since the data can be more rapidly accessed from the higher speed storage device." (Col 1, Line 18)]** "a write director coupled to the storage mechanism and to the at least one local storage cache for controlling content written into the storage mechanism and to the at least one local storage cache" **[Chiou et al. discloses this limitation as "A cache manager software program may be executed by a processor on this card and the manager may monitor the data traffic through the system and manage the local cache." (Col 3, Line 53)]** "a cache manager for managing content copying between the storage mechanism and the at least one local storage cache to maintain at least partial content coherency" **[Chiou et al. discloses this limitation as "To maintain the cache coherency, a user configurable cache scheme will be used to customize the implementation of the system which implements sophisticated cache algorithms." (Col 6, Line 33) and "However, when a write request occurs, the system on the storage side will use the written data to refresh its cache and the cache system on the host side will either use the data to refresh its cache or to simply invalidate the same data in the cache if it was already there. Moreover, the system on the host side will work with all other cache systems on the network that are on the same access zone to do the same update or invalidation operations for their caches." (Col 3, Line 24)]** "a read

director responsive to a request for content from a user for directing said content request to a selected one of the at least one local storage cache and the storage mechanism depending on content availability of each" **[Chiou et al. discloses this limitation as "Each read request initiated by a host would first be checked against the cached data in host-side cache system and be satisfied by that system if the requested data is present. If the host-side cache could not satisfy the read request, the read request is sent out to the storage-side cache. If a cache hit occurs at the storage-side cache system, the read request is satisfied by that system. If both cache systems fail to generate a cache hit for the read request then the request is forwarded to the target storage device to satisfy the read request." (Col 3, Line 3)]** "a storage mechanism access manager for monitoring read and write loading of the storage mechanism and for controlling the read and write directors and the cache manager in accordance with the storage mechanism read and write loading." **[Chiou et al. discloses this limitation as "a cache unit for caching data between a computer host and a storage device is provided. The cache unit comprises a computer host cache for caching data requested by the computer host, a storage device cache for caching data stored on the storage device, and a cache controller for servicing the read and write requests from the computer host for data located on the storage device." (Col 5, Line 11)]** "wherein controlling the write directors includes reducing writing to the storage mechanism" [**"In the "critical coherent" mode, the cache gets updated or invalidated before the data gets actually written to the target device." (Col 15, Lines 3-5) and "The first is a strict**

synchronous mode (critical coherent mode) which does not forward the write request until all caches have been either updated or invalidated. The second is non-critical coherent mode which would execute the update or invalidation in parallel with performing the write." (Col 9, Lines 24-29)].

As per Claim 2, Chiou et al discloses, "wherein the cache manager manages the storage capacity of the local cache storage unit by successively deleting a least accessed file until the local cache storage unit has an available storage capacity above a prescribed level" as **["In step 98, the cache manager may check for available space in the SSC cache to see if, to store the current requested data, the cache manager needs to purge old cache data using either a typical least recently used cache data replacement algorithm or alternatively using pre-set time limits depending on their data types." (Col 13, Line 29)].**

As per Claim 4, Chiou et al discloses, "wherein the storage mechanism further comprises at least one disk drive" as **["each computer system 24 may include one or more computer/storage systems 26, such as servers or disk-based RAID controllers" (Col 7, Line 32)].**

As per Claim 5 & 7, Chiou et al. discloses, "wherein the storage mechanism further comprises at least one Redundant Array of Inexpensive Disk Drives (RAID)" as **["each computer system 24 may include one or more computer/storage systems 26, such as servers or disk-based RAID controllers" (Col 7, Line 32)].**

As per Claim 6, Chiou et al. discloses, "wherein the local cache storage unit further comprises at least one disk drive" as **["The cache memory, in accordance**

with the invention, may be either solid-state memory or magnetic-mechanical type disk drives." (Col 6, Line 38)].

As per Claim 8, Chiou et al. discloses, "wherein the read director redirects a request for content to the local cache storage unit when the requested content is available at the local cache storage unit to reduce bandwidth requirements on the storage mechanism" as **["The cache system will shorten the access time versus the available network bandwidth, if the accessed data is hit in the cache." (Col 6, Line 32)].**

As per Claim 9, Chiou et al. discloses, "wherein the cache manager copies at least some content from the storage mechanism to the local cache storage unit previously unavailable on the local cache storage unit" as **["If a cache hit does not occur (e.g., the requested data is not located in the SSC cache), then the line card reads the requested data from the target disk and sends the data back to the requestor in step 94. In step 96, the line card may forward the requested data along with the original request to the cache manager responsible for the target device. In step 98, the cache manager may check for available space in the SSC cache to see if, to store the current requested data" (Col 13, Line 18)].**

As per Claim 10, Chiou et al. discloses, "wherein the storage mechanism access manager controls the read and write directors to reduce reading from, and writing to the storage mechanism during intervals of limited storage mechanism bandwidth" as **["The type of caching may be either file-based caching or block-based caching. A file caching implementation, in accordance with the invention, allows the cached data**

to exist in the host-side system or storage-side system, but the data may also be located anywhere inside the storage network infrastructure. Therefore, as long as the system maintains a fast locator for the cached file data, the physical location of the file data is irrelevant. The block caching implementation allows the cached data to be stored in the host-side system or the storage-side system and eliminates the need to access the data across bandwidth limited LAN, SAN or WAN networks." (Col 6, Line 40)].

As per Claim 11, Chiou et al. discloses, "writing incoming content to at least one of a Storage Area Network (storage mechanism) and a local cache storage unit" as **[See figures 7-9. "In step 196, after the cache has been updated or invalidated, the line card sends a write request and the data to the target device." (Col 15, Line 20)]** "monitoring content coherency between the storage mechanism and the local cache storage unit" **[Chiou et al. discloses this limitation as "To maintain the cache coherency, a user configurable cache scheme will be used to customize the implementation of the system which implements sophisticated cache algorithms." (Col 6, Line 33)]** "copying content between the storage mechanism and the local cache storage unit in accordance with the content coherency there between" **[Chiou et al. discloses this limitation as "However, when a write request occurs, the system on the storage side will use the written data to refresh its cache and the cache system on the host side will either use the data to refresh its cache or to simply invalidate the same data in the cache if it was already there. Moreover, the system on the host side will work with all other cache systems on the network**

that are on the same access zone to do the same update or invalidation operations for their caches." (Col 3, Line 24)] "directing a request for content from a user to a selected one of the storage mechanism and the local cache storage unit depending on the content availability of each" **[Chiou et al. discloses this limitation as "Each read request initiated by a host would first be checked against the cached data in host-side cache system and be satisfied by that system if the requested data is present. If the host-side cache could not satisfy the read request, the read request is sent out to the storage-side cache. If a cache hit occurs at the storage-side cache system, the read request is satisfied by that system. If both cache systems fail to generate a cache hit for the read request then the request is forwarded to the target storage device to satisfy the read request." (Col 3, Line 3)]** "monitoring read and write loading of the storage mechanism; and controlling reading of content from, and writing of content to the storage mechanism in accordance with the storage mechanism read and write loading." **[Chiou et al. discloses this limitation as "a cache unit for caching data between a computer host and a storage device is provided. The cache unit comprises a computer host cache for caching data requested by the computer host, a storage device cache for caching data stored on the storage device, and a cache controller for servicing the read and write requests from the computer host for data located on the storage device." (Col 5, Line 11)]** "wherein controlling the write directors includes reducing writing to the storage mechanism" [**"In the "critical coherent" mode, the cache gets updated or invalidated before the data gets**

actually written to the target device." (Col 15, Lines 3-5) and "The first is a strict synchronous mode (critical coherent mode) which does not forward the write request until all caches have been either updated or invalidated. The second is non-critical coherent mode which would execute the update or invalidation in parallel with performing the write." (Col 9, Lines 24-29)].

As per Claim 12, Chiou et al. discloses, "wherein the step of directing the content request further comprises re-directing the content request to the local cache storage unit if the requested content resides at the local cache storage unit" **["The cache system will shorten the access time versus the available network bandwidth, if the accessed data is hit in the cache." (Col 6, Line 32)].**

As per Claim 15, Chiou et al. discloses, "comprising the step of writing content from the local cache storage unit to the storage mechanism" as **["In the "critical coherent" mode, the cache gets updated or invalidated before the data gets actually written to the target device." (Col 15, Line 3)].**

As per Claim 16, Chiou et al. discloses, "wherein the step of controlling reading of content from, and writing of content to the storage mechanism further comprises the step of restricting access to the storage mechanism during intervals of high bandwidth demand" as **["The type of caching may be either file-based caching or block-based caching. A file caching implementation, in accordance with the invention, allows the cached data to exist in the host-side system or storage-side system, but the data may also be located anywhere inside the storage network infrastructure. Therefore, as long as the system maintains a fast locator for the cached file data,**

the physical location of the file data is irrelevant. The block caching implementation allows the cached data to be stored in the host-side system or the storage-side system and eliminates the need to access the data across bandwidth limited LAN, SAN or WAN networks." (Col 6, Line 40)].

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. **Claims 3, 13-14** are rejected under 35 U.S.C. 103(a) as being unpatentable over Chiou et al. (United States Patent 6,792,507) in view of Tremblay et al. (United States Patent Application Publication US 2002/0184460 A1).

As per Claim 3 & 13, Chiou et al. discloses, "The storage system of claim 1" as **[See rejection to Claim 1 above]** "insufficient bandwidth exists to access the storage mechanism" **["The cache manager is responsible for monitoring the data traffic" (Col 11, lines 26-32) and "sending the data to all HSC cache systems on the network for cache data update may create congestion in network traffic" (Col 8, Lines 60-62)],** but fails to explicitly disclose "further comprises a filler storage unit for storing filler content, and wherein the read director directs the read request to the filler storage unit to provide filler content when the requested content is unavailable from the storage mechanism and the local storage cache unit."

Tremblay et al. discloses, "further comprises a filler storage unit for storing filler content, and wherein the read director directs the read request to the filler storage unit to provide filler content when the requested content is unavailable from the storage mechanism and the local storage cache unit" as **["The store pair transaction generated from the received store pair instruction includes (1) a write command to write data in main memory; (2) one beat of data to be written in main memory and three beats of unused or filler data; (3) byte enable information specifying which bytes of the one beat of data is to be actually written in memory" (Paragraph 0027)]**

Chiou et al and Tremblay et al. are analogous art because they are all from the same field of endeavor of accessing memory and storage.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify the system of Chiou et al to include the use of filler data to fill in data where data is not available as disclosed by Tramblay et al. Chiou et al. discloses the availability of a second level of cache in the client computer. In combination with the filler data disclosed by Tramblay et al., they disclose the invention claimed. The motivation to combine these arts is found in Tramblay et al. as "Cache memory is configured to transfer data to and from memory controller in bursts and provide access to stored data to load/store unit. In a preferred embodiment, cache memory 130 organizes and stores data according to cache lines. In one embodiment, a cache line comprises four 8-byte words or beats." (Paragraph 0028) As data is provided in bursts, filler data must be used to cover where data is unavailable.

Therefore it would have been obvious to combine the teachings of Chiou et al. with Tremblay et al. to obtain the inventions claimed in **Claim 3 & 13.**

As per Claim 14, Chiou et al and Tremblay et al. further disclose, "comprising the step of writing content from the storage mechanism to the local cache storage unit" as **["If a cache hit does not occur (e.g., the requested data is not located in the SSC cache), then the line card reads the requested data from the target disk and sends the data back to the requestor in step 94. In step 96, the line card may forward the requested data along with the original request to the cache manager responsible for the target device. In step 98, the cache manager may check for available space in the SSC cache to see if, to store the current requested data" (Col 13, Line 18)].**

(10) Response to Argument

Appellants allege:

(a) Claims 1 and 11 are patentable over Chiou, as Chiou fails to anticipate the feature of reducing writing on a storage mechanism in accordance with read and write loading on the storage mechanism.

(b) Claims 3 and 13 are patentable over Chiou in view of Tremblay, as neither reference renders obvious the feature of providing filler content as a substitute for real data.

With respect to (a), Examiner appreciates the interpretative description given by Appellants in response. Appellants' specification discloses a system that comprises “A cache manager manages the content coherency between the storage mechanism and the local cache storage unit so that at least some of the content on the storage mechanism also exists on the local cache storage unit and vice versa.” (Paragraph 0005) where “the write director 16 directs incoming content to either or both of the storage mechanism 12 and the local cache storage unit 14.” (Paragraph 0009). Additionally, “The local cache storage unit 14 serves to mirror at least some of the content on the storage mechanism 12, thus providing an alternate source for supplying such content to a user.” (Paragraph 0012). “To accomplish this task, … the cache manager 18 undertakes background copying of files to the storage mechanism 12 from the local cache storage unit 14 ("trickle up"). Such trickle up becomes necessary when a user edits content for subsequent use by others. The rate at which "trickling down" and "trickling up" occurs is a function of the overall bandwidth demand on the storage mechanism 12.” (Paragraph 0010).

According to this system, incoming traffic can be directed to the cache or to the storage mechanism or both. Coherency between the cache and storage must be managed so that the local cache mirrors at least some of the content of the storage. Further, the method to which data can be copied from the cache to the storage is through a “trickle up", which the Appellants claim is reducing writing to the storage in accordance with the read and write loading, as the data is copied to the cache first then

"trickled up" to the storage. The writing to the storage is reduced during the period of initial loading of the cache from the input to the system and spread across the “trickle up” period.

In the above stated claims, some of the recited features of the Appellants claims are: “a storage mechanism access manager for monitoring read and write loading of the storage mechanism and for controlling the read and write directors and the cache manager in accordance with the storage, mechanism read and write loading, wherein controlling the write directors includes reducing writing to the storage mechanism".

The Appellants' disclosure, as pointed out above, states that the when a user edits content for subsequent use by others that data must be “trickled up” to the storage server. As the claims do not contain any particular identification of data type, it is interpreted that all data/content is of the 'trickle-up' required type. (Claim 1: “reducing writing to the storage mechanism”). The disclosure does not further recite specifics or limitations with regards to the "trickle-up" or “reducing writing" beyond “The rate at which "trickling down" and "trickling up" occurs is a function of the overall bandwidth demand on the storage mechanism 12.” (Paragraph 0010). Similarly the claims do not produce a limitation on the trickle up rate of the data from the cache to the storage mechanism, rather that only "writing to the storage is reduced". Therefore, in the interpretation of the examiner based on the reasonable interpretation of one of ordinary skill in the art of the Appellants’ Claims and specifications (reading in light of the specifications by without drawing limitations of the specifications into the claims), the reducing of writing to the

storage mechanism occurs by delaying the incoming data from writing to the storage mechanism, by first loading it to the cache, then loading it to the storage mechanism.

Chiou system discloses, “In the "critical coherent" mode, the cache gets updated or invalidated before the data gets actually written to the target device.” (Col 15, Lines 3-5) and “The first is a strict synchronous mode (critical coherent mode) which does not forward the write request until all caches have been either updated or invalidated. The second is non-critical coherent mode which would execute the update or invalidation in parallel with performing the write.” (Col 9, Lines 24-29)].

The claims require the storage mechanism access manager to monitor read and write loading. Examiner continues to assert that Chiou does teach a mechanism that monitors the read and write requests on a main storage unit. Chiou teaches: “The cache manager is responsible for monitoring the data traffic, mapping data into the cache storage, purging data from the cache memory when it becomes full, and updating the cache tag tables. It accomplishes these tasks by working closely with the local line card control processes as well as cache managers running on other cache systems on the network.” (Col 11, lines 26-32).

The claims also require the storage mechanism access manager for controlling the read and write directors and the cache manager in accordance with the storage mechanism read and write loading. The Examiner notes that the “in accordance with the storage mechanism read and write loading" is NOT a limitation whereby requiring the manager to act "in accordance with the **monitored** read and write loading". It is very well known in the art that read and write loading can be determined in many different

ways. The file or block caching system of Chiou, when used in conjunction with the “The first is a strict synchronous mode (critical coherent mode) which does not forward the write request until all caches have been either updated or invalidated.” (Col 9, Lines 24-29), reduce the number of writes during an interval, by restricting them to occur at a later time. Chiou discloses, “Two options with respect to write cache update or cache invalidation are offered to the user depending on the user's configuration. The first is a strict synchronous mode (critical coherent mode) which does not forward the write request until all caches have been either updated or invalidated. The second is non-critical coherent mode which would execute the update or invalidation in parallel with performing the write. The non-critical coherent mode **could be used in static web page servers where delayed invalidations would not matter as occasionally stale reads would be rare and would not be critical to the viewer of the web page**.” (Col 9, Line 22-33). Chiou clearly discloses, where the user selects the mode based on the type of application the invention will be used it within based on the importance to prevent "static reads" versus "critical write" which are functions of read and write loading. Appellants' claims do not require the storage access manager to automatically and selectively choose to reduce writing, but rather that it is based on read write loading, including controlling the writing directors to reduce writing. Chiou discloses this by having the user select the mode based on the storage mechanism read and writing loading. It is clear that the user would configure the system based on which option would be appropriate for their setup based on read and write loading (type of read and write requests), which is in accordance to the definition provided by Appellants in

response filed June 7, 2007 “One of ordinary skill in the art would recognize that monitoring the read and write load on the storage mechanism includes monitoring **the number and type of the read and write requests**" (Page 8, 1st paragraph).

With respect to (b), Examiner appreciates the interpretative description given by Appellants in response. Appellants' specification discloses a system that comprises “If the content does not reside on the local cache storage unit, read director directs the request to the storage mechanism, but if the content is unavailable, the content request will be filled with filler data from a filler data source.” (Abstract) “a storage unit 24 provide the user with filler content in the event the local cache storage unit 14 can not provide the requested content and insufficient bandwidth exists to permit access to the storage mechanism 12.” (Paragraph 0011) “a filler storage unit for storing filler content, and wherein the read director directs the read request to the filler storage unit to provide filler content when the requested content is unavailable from the storage mechanism and the local storage cache unit.” (originally filed claim 3).

Accordingly to this system as disclosed, a filler storage stores filler content and provides filler content to a request if the local cache cannot provide the requested content and access is not permitted (due to bandwidth) to the storage mechanism.

Tremblay discloses, “In one embodiment, the instruction combining logic receives write transactions generated from store pair instructions, stores data from the write transactions in a buffer, and combines the data in the buffer. The combined data is

subsequently written to memory in a single write transaction. The instruction combining logic may determine whether the data from the transactions are in the same cache line before combining them. A programmable timer may be used to measure the amount of time that has elapsed after the instruction combining logic receives the first write transaction. If the elapsed time exceeds a predetermined limit before another write instruction is received, the instruction combining logic combines the data in the buffer and writes it to memory in a single write transaction." (Abstract).

Examiner points out that the Appellants' claims do not point out the limitation of "filler data is a substitute for real data". Regardless, Tremblay does substitute filler data for real data, as the Appellants points out. Appellants states that Tremblay "states that in one embodiment of its system, "**the format** of the memory store instruction.., includes: (1) a write command; (2) **four beats of data**"" then states "store pair instruction includes: "(1) a write command to write data in main memory; (2) one beat of data to be written in main memory and three beats of unused or filler data;" (Page 12 of Response). The filler data is substituting for the real data of "four beats of data", where one beat is real data and three beats are filler data, in order to complete the format stated above.

Tremblay uses the filler beats to "follow the general format" or substitute filler data for real data so the format is maintained. "The invention, however, may be applied to other types of memory access instructions, such as instructions to write more than one beat of data in main memory, instructions to write data to the cache memory, and instructions to read data." Paragraph 0026. The format has beats available if the

instruction can write more than one beat, but uses filler data when such beats are unavailable for the current instruction. Further the disclosure only provides for "filler content" to be provided. It does not claim or disclose that what this filler content may be.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,
Kenneth M. Lo
Examiner
Art Unit 2188

Conferees:

/Hyung S SOUGH/

Supervisory Patent Examiner, Art Unit 2188

/Manorama Padmanabhan/

Quality Assurance Specialist, TC2100, WG 2180